(Features

- Low-voltage and Standard-voltage Operation
  - 1.8 (V_{CC} = 1.8 to 5.5V)
- Internally Organized 4096 x 8, 8192 x 8
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bi-directional Data Transfer Protocol
- 1 MHz (5.0V) and 400 KHz (1.8V Compatibility)
- Write Protect Pin for Hardware Data Protection
- 32-Byte Page Write Mode (Partial Page Writes Allowed)
- Self-Timed Write Cycle (5 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Lead-free/Halogen-free Devices
- 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Lead Frame Land Grid Array (ULA), 8-lead TSSOP, 8-lead Ultra Thin Mini-MAP (MLP2x3), and 8-ball dBGA2 Packages.
- Die Sales: Wafer Form, Waffle Pack, and Bumped Wafers

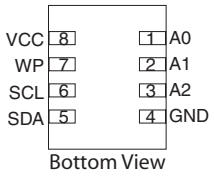
Description

The AT24C32C/64C provides 32,768/65,536 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 4096/8192 words of 8 bits each. The device's cascadable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C32C/64C is available in space saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Lead Frame Land Grid Array (ULA), 8-lead TSSOP, 8-lead Ultra Thin Mini-MAP (MLP2x3) and, 8-ball dBGA2 packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 1.8V (1.8 to 5.5V) version.

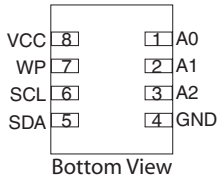
Pin Configurations

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

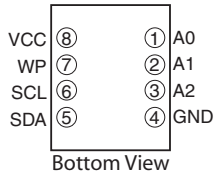
8-lead Ultra Thin Mini-MAP (MLP 2x3)



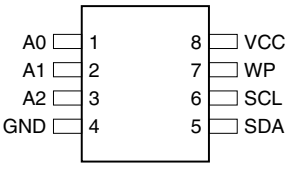
8-lead Ultra Lead Frame Land Grid Array (ULA)



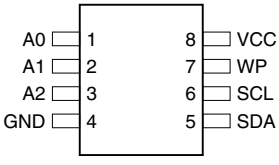
8-ball dBGA2



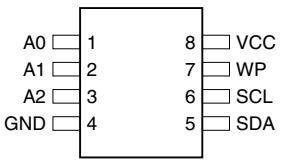
8-lead TSSOP



8-lead SOIC



8-lead PDIP



2-Wire Serial EEPROM

32K (4096 x 8)

64K (8192 x 8)

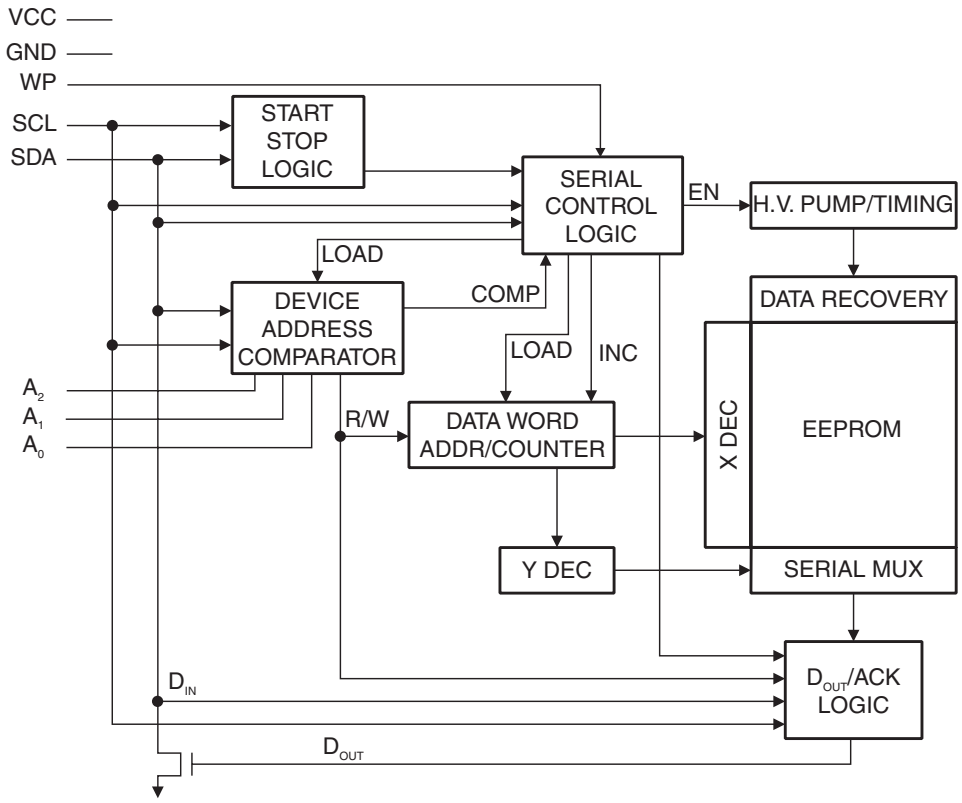
AT24C32C
AT24C64C

Absolute Maximum Ratings*

Operating Temperature	-55 to +125°C
Storage Temperature	-65 to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Block Diagram



3. Memory Organization

AT24C32C/64C, 32/64K SERIAL EEPROM: The 32K/64K is internally organized as 128/256 pages of 32 bytes each. Random word addressing requires a 12/13 bit data word address.

Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V to 5.5V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40 to +85°C, V_{CC} = +1.8 to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V	READ at 400 kHz		0.4	1.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V	WRITE at 400 kHz		2.0	3.0	mA
I_{SB1}	Standby Current (1.8V option)	V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}			1.0	µA
		V_{CC} = 5.5V				6.0	µA
I_{LI}	Input Leakage Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current V_{CC} = 5.0V	V_{OUT} = V_{CC} or V_{SS}			0.05	3.0	µA
V_{IL}	Input Low Level[1]			–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level	V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level	V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	1.8-volt		5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3		0.4		µs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		µs
t_i	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.05	0.9	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1.3		0.5		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		µs
$t_{SU.STA}$	Start Set-up Time	0.6		0.25		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		100		ns
t_R	Inputs Rise Time(1)		0.3		0.3	µs
t_F	Inputs Fall Time(1)		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		0.25		µs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance(1)	25°C, Page Mode, 3.3V	1,000,000				Write Cycles

Notes: 1. This parameter is ensured by characterization.

2. AC measurement conditions:
   R_L (connects to V_{CC}): 1.3 kΩ (2.5V, 5.0V), 10 kΩ (1.8V)
   Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
   Input rise and fall times: ≤ 50 ns
   Input and output timing reference voltages: 0.5 V_{CC}

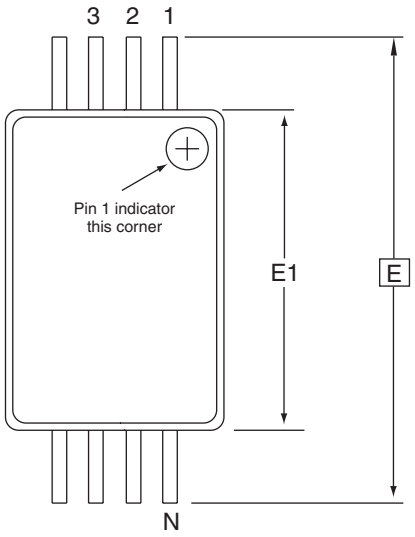
AT24C64C Ordering Information

Ordering Code	Voltage	Package	Operation Range
AT24C64C-PU (Bulk form only)	1.8	8P3	Lead-free/Halogen-free Industrial Temperature (-40°C to 85°C)
AT24C64CN-SH-B[1] (NiPdAu Lead Finish)	1.8	8S1	
AT24C64CN-SH-T[2] (NiPdAu Lead Finish)	1.8	8S1	
AT24C64C-TH-B[1] (NiPdAu Lead Finish)	1.8	8A2	
AT24C64C-TH-T[2] (NiPdAu Lead Finish)	1.8	8A2	
AT24C64CY6-YH-T[2] (NiPdAu Lead Finish)	1.8	8Y6	
AT24C64CD3-DH-T[2] (NiPdAu Lead Finish)	1.8	8D3	
AT24C64CU2-UU-T[2]	1.8	8U2-1	
AT24C64C-W-11[3]	1.8	Die Sale	Industrial Temperature (-40°C to 85°C)

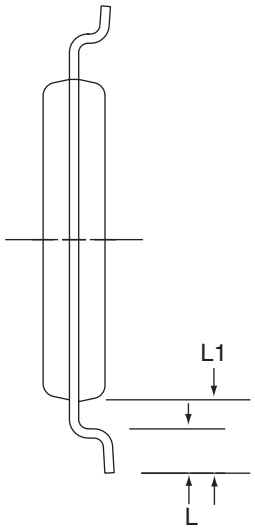
Notes: 1. "-B" denotes Bulk.
2. "-T" denotes tape and reel. SOIC = 4K per reel. TSSOP, Ultra Thin Mini-MAP and dBGA2 = 5K per reel.
3. Available in waffle pack, tape and reel, and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Interface Marketing.

Package Type	
8Y6	8-lead, 2.00mm x 3.00mm Body, 0.50mm Pitch, Ultra Thin Mini-MAP, Dual no Lead Package (DFN), (MLP 2x3)
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 4.4 mm Body, Plastic, Thin Shrink Small Outline Package (TSSOP)
8U2-1	8-ball, die Ball Grid Array Package (dBGA2)
8D3	8-lead, 1.80 mm x 2.20 mm Body, Ultra Lead Frame Land Grid Array (ULA)
Options	
-1.8	Low Voltage (1.8V to 5.5V)

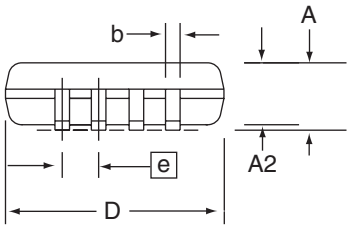
8A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8A2**, 8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	8A2	B